Claims

What is claimed is:

1. A system, comprising:

a first delay circuit configured for programmably delaying a strobe signal with a first delay to latch a data signal; and

a second delay circuit configured for delaying the data signal with a second delay that is substantially inherent to the first delay circuit.

2. The system of claim 1, further comprising a logic circuit communicatively coupled between the first and the second delay circuits and configured for latching the data signal substantially aligned with the strobe signal.

3. The system of claim 2, wherein the logic circuit comprises a flip/flop device.

4. The system of claim 1, further comprising a master delay circuit configured for locking a clock signal and for programming the first delay circuit with the first delay therefrom.

5. The system of claim 4, wherein the second delay comprises a duration that is less than a cycle duration of the clock signal.

6. The system of claim 1, further comprising a plurality of the first and the second delay circuits.

7. The system of claim 1, wherein the first and the second delay circuits comprise substantially the same integrated circuitry such that the first delay circuit comprises a first overhead substantially having the second delay and the second delay circuit comprises a second overhead having the second delay.

8. A method of latching a data signal, comprising steps of:

programmably delaying a strobe signal with a first delay;

delaying the data signal with a second delay that is inherently produced by the step of programmably delaying; and

registering the data signal responsive to the first delay using the strobe signal.

9. The method of claim 8, further comprising a step of locking a clock signal to generate a control signal that programmably delays the strobe signal with the first delay.

10. The method of claim 9, wherein the step of locking comprises a step of simultaneously transferring the control signal through a plurality of control lines to uniformly perform the step of programmably delaying.

11. The method of claim 8, wherein the step of delaying the data signal comprises a step of generating the second delay such that the duration of the second delay is less than a cycle duration of the clock signal.

12. The method of claim 8, wherein the step of registering the data signal comprises steps of:

receiving the data signal; and

latching the data signal with the strobe signal.

13. A system for latching a data signal, comprising:

means for programmably delaying a strobe signal with a first delay;

means for delaying the data signal with a second delay that is inherently produced by the means for programmably delaying; and

means for registering the data signal responsive to the first delay using the strobe signal.

14. The system of claim 13, further comprising means for locking a clock signal to generate a control signal that programmably delays the strobe signal with the first delay.

15. The system of claim 14, wherein the means for locking comprises means for simultaneously transferring the control signal through a plurality of control lines to uniformly perform the means for programmably delaying.

16. The system of claim 13, wherein the means for delaying the data signal comprises means for generating the second delay such that the duration of the second delay is less than a cycle duration of the clock signal.

17. The system of claim 13, wherein the means for registering the data signal comprises:

means for receiving the data signal; and

means for latching the data signal with the strobe signal.

18. A system, comprising:

a first delay circuit configured for programmably delaying a first signal with a first delay to provide a delayed first signal; and

a second delay circuit configured for delaying the first signal with a second delay that is substantially inherent to the first delay circuit to latch the delayed first signal

19. The system of claim 18, further comprising monitor logic communicatively coupled between the first and the second delay circuits and configured for latching the delayed first signal in substantially alignment with the first signal.

20. The system of claim 19, wherein the monitor logic is further adapted to provide timing for the system that corresponds with the first signal and to program the first delay circuit with the first delay therefrom.

21. The system of claim 18, wherein the second delay comprises a duration that is less than a cycle duration of the first signal.

22. The system of claim 18, further comprising a plurality of the first and the second delay circuits.

23. The system of claim 18, wherein the first and the second delay circuits comprise substantially the same integrated circuitry such that the first delay circuit comprises a first overhead delay substantially having the second delay and the second delay circuit comprises a second overhead delay having the second delay.